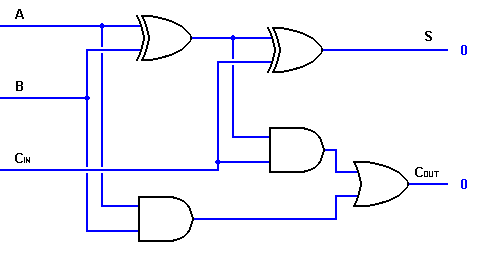
**Circuit Diagram & Truth Table:**



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Cin** | **a** | **b** | **sum** | **Cout** |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**Code:**

* **Design Module**

module obfa(sum,cout,a,b,cin);

input a,b,cin;

output sum,cout;

wire x,y,z;

xor(x,a,b);

xor(sum,x,cin);

and a1(y,x,cin);

and a2(z,a,b);

or o1(cout,y,z);

endmodule

* **TestBench**

module baig;

reg a,b,cin;

wire sum,cout;

obfa g1(sum,cout,a,b,cin);

initial

begin

a=1'b0;b=1'b0;cin=1'b0;

#20

a=1'b0;b=1'b1;cin=1'b1;

#20

a=1'b1;b=1'b0;cin=1'b1;

#20

a=1'b1;b=1'b1;cin=1'b1;

#20

$finish;

end

endmodule

**Output:**

Graphical user interface, text, application

Description automatically generated